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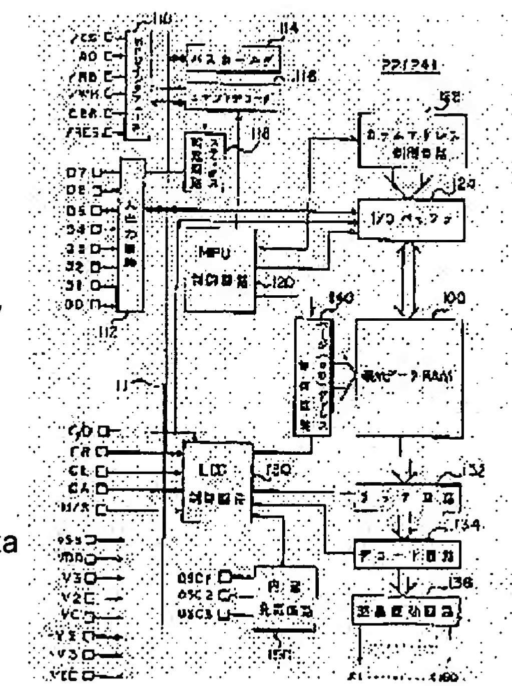
(71)Applicant : **SEIKO EPSON CORP**

(72)Inventor : **ISOZAKI SHINGO**

(54) LIQUID CRYSTAL DRIVE DEVICE AND SIGNAL ELECTRODE DRIVE CIRCUIT



(57)Abstract:

PROBLEM TO BE SOLVED: To reduce electric power consumption and perform liquid crystal drive capable of changing over gradation display and binary display of two times the number of display picture elements by constituting a signal electrode driving circuit (column driver) so as to have a frame memory for storing display data and a gradation display control means.

SOLUTION: A column driver is provided with first and second signal line drive IC. This signal line driver IC is provided with a display data RAM 100, a MPU control circuit 120 controlling read/write operation of display data for the display data RAM 100 at one bite unit for example, and a LCD control circuit 130 controlling to read out display data of four lines for example from the display data RAM 100 and capable of driving MLS (multi-line-selection) of four-line simultaneous selection. By operating readout of every L bits, electric power consumption is reduced, and liquid crystal capable of changing over gradation display and binary display of two times the number of display picture elements can be driven.

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CLAIMS

[Claim(s)]
[Claim 1] The liquid crystal driving gear with which a signal-electrode drive circuit is characterized by having the frame memory and gradation display-control means for indicative-data storage in the liquid crystal driving gear which consists of a scanning electrode drive circuit and a signal-electrode drive circuit, and performs the display control by the two or more line simultaneous selection driving method.
[Claim 2] It is the liquid crystal driving gear with which a liquid crystal driving gear according to claim 1 has the number of gradation of the m-th power of 2, and a 1-pixel indicative data is characterized by the bird clapper from m bits.
[Claim 3] It is the signal-electrode drive circuit characterized by reading L bits at a time in case the composition which makes the display RAM of 2L bit correspond to the processing circuit which generates 1 segment output will be taken and RAM read-out operation for liquid crystal driving-signal determination will be performed in the signal-electrode drive circuit of a liquid crystal driving gear according to claim 1, if the number of simultaneous selection lines is set to L.
[Claim 4] A liquid crystal driving gear according to claim 1 is a liquid crystal driving gear characterized by having a gradation display-control means.
[Claim 5] A liquid crystal driving gear according to claim 4 is a liquid crystal driving gear characterized by performing the gradation display control by PDM.
[Claim 6] A liquid crystal driving gear according to claim 5 is a liquid crystal driving gear characterized by the length of pulse width being adjustable.
[Claim 7] A liquid crystal drive circuit according to claim 1 is a liquid crystal driving gear characterized by the gradation display of the m-th power and binary display of 2 being switchable, and a display m times the number of lines of the number of the maximum lines in a gradation display being possible in case it is a binary display.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to improvement of the liquid crystal driving gear used for a liquid crystal display.
[0002]
[Description of the Prior Art] Conventionally, in the simple matrix liquid crystal display as an example of a flat-panel display, the method using a matrix type liquid crystal display element module controller (henceforth a module controller) as a method which transmits an indicative data to a LCD module (it consists of a liquid crystal display panel, a scanning electrode drive circuit, a signal-electrode drive circuit, etc.) from the MPU (microprocessor unit) side is typical. This method reads an indicative data from the Video RAM (VRAM) the module controller connected with a system bus like the display which used CRT has remembered the indicative data to be, transmits this with the clock of high frequency to a LCD module, and display refreshment operation is performed. In case a gradation display is performed in such a LCD module, usually, a module controller performs a gradation display control, changes into a binary signal to a signal-electrode drive circuit, and the indicative data is transmitted.
[0003]
[Problem(s) to be Solved by the Invention] However, since read-out from a video ram (it is called Following VRAM) and a transfer are performed in accordance with liquid crystal display timing, in the above-mentioned conventional example, it is usually necessary to always operate VRAM, a module controller, and a liquid crystal driver by the high-frequency clock of several MHz, and to have a RF generating circuit for it in a module controller. Moreover, penetration current etc. arises in much CMOS with which VRAM, a module controller, and a liquid crystal driver are covered, and the circuit related to this operation of a series of constitutes a circuit element according to operation of the large-scale circuit in this high-frequency clock, and it leads to increase of power consumption, and if a large-sized LCD panel is used, it will increase so much. Furthermore, since a transfer clock goes up as compared with a binary display when performing a gradation display, the further increase of power consumption is caused.
[0004] Then, it is that the purpose of this invention improves handling and gradation display control of the indicative data for a gradation display in view of the above-mentioned trouble, and though it is a low power, it is in offering the easy liquid crystal driving gear of an equipment configuration.
[0005]
[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the means which this invention provided builds in display memory in a signal-electrode drive circuit (column driver), and is characterized by the form to which the column driver was made to carry out the gradation display control itself.
[0006]
[The form of operation of this invention] Hereafter, this invention is concretely explained with reference to a drawing about the form of operation of the adapted liquid crystal driving gear.

[0007] (Explanation of the control system of the whole equipment) Drawing 1 shows the general drawing of the liquid crystal driving gear containing a liquid crystal display panel. In drawing 1 , the liquid crystal display panel 10 is equipped with the pixel of 320x240, a switching element and a liquid crystal layer are connected to the pixel position formed of intersection with 320 signal lines and the 240 scanning lines in series, and a pixel is constituted. In addition, let the liquid crystal display panel 10 be the active matrix type liquid crystal display panel which connected to each liquid crystal layer of a pixel position 3 terminal type switching element represented with TFT, or 2 terminal type switching element represented by MIM. Or you may be a simple matrix type liquid crystal display panel.
[0008] The liquid crystal driving gear for driving this liquid crystal display panel 10 consists of the signal-line driver 20, the scanning-line driver 30, a power circuit 40, and an external circuit 50 for an oscillation. The aforementioned signal-line driver (column driver) 20 supplies a data signal to 320 signal lines, and has the 1st signal-line drive IC 22 and the 2nd signal-line drive IC 24 in this example. The 1st signal-line drive IC 22 supplies a data signal to one to 160 Motome's signal line, and the 2nd signal-line drive IC 24 supplies a data signal to 161 to 320 Motome's signal line. In addition, in this example, a cascade connection is possible for four signal-line drives IC, and they can drive 160x4=640 signal line at the maximum.
[0009] The this 1st [the] and 2nd signal-line drive 22 and ICs 24 has [both] the same composition. In order to use properly a maximum of four signal-line drives IC in which a cascade connection is possible in step [1st] - the 4th step, two external terminals, LR0 and LR1, are prepared in each IC, and the combination of the potential impressed to the external terminal is changed. The 1st signal-line drive IC 22 of the 1st step is set as LR0 terminal =LR1 terminal =L, and the 2nd signal-line drive IC 24 of the 2nd step is set as LR0 terminal =L and LR1 terminal =H. Although drawing 1 does not show, the 3rd-step signal-line drive IC is set as LR0 terminal =H and LR1 terminal =L, and the 4th-step signal-line drive IC is set as LR0 terminal =H and LR1 terminal =H.
[0010] The scanning-line driver (low driver) 30 supplies a scanning signal to the 240 scanning lines, and has the 1st scanning-line drive IC 32 and the 2nd scanning-line drive IC 34 in this example. The 1st scanning-line drive IC 32 supplies a scanning signal to one to 120 Motome's scanning line, and the 2nd scanning-line drive IC 34 supplies a scanning signal to 121 to 240 Motome's scanning line.
[0011] Power is supplied to the signal-line driver 20 and the scanning-line driver 30 from a power circuit 40, and various command signals and a data signal are supplied to them from a microprocessing unit (MPU) 60.
[0012] (Explanation of the signal-line drive IC) Next, the detail of the 1st which both has the same composition, and 2nd signal-line drive 22 and ICs 24 is explained with reference to drawing 2 .
[0013] Drawing 2 shows composition common to the signal-line drive IC. With indicative-data RAM100 and the MPU control circuit 120 which controls read/write operation of an indicative data per 1 byte as opposed to this indicative-data RAM100, from indicative-data RAM100, the indicative data for four lines is read and controlled, and this signal-line drive IC has the LCD control circuit 130 which enables the MLS (multi-line selection) drive of four-line simultaneous selection. /CS, A0, /RD, /WR, C86, and /RES are connected to the bus line 111 inside IC through the MPU interface 110 as a terminal for bus connections. Moreover, D7-D0 are further connected to this bus line 100 through the I/O circuit 112 as a terminal for bus connections. The control data and the indicative data which are outputted and inputted through the MPU interface 110 and the I/O circuit 112 can be held by the bus holder 114 through a bus line 111. Control data is decoded by the command decoder 116, and is used as a command signal to the status setting circuit 118 and the MPU control circuit 120.
[0014] The MPU control circuit 120 controls the column address control circuit 122 and I/O buffer 124 for RAM, and carries out read/write of the indicative data to RAM100 per 1 byte.
[0015] Moreover, it connects with external terminal G/D, FR, CL and CA, and M/S, and the LCD control circuit 130 is connected with the internal oscillator circuit 150. This LCD control circuit 130 carries out drive control of a latch circuit 132 and the decoding circuit 134, reads the indicative data for four lines from RAM100, and supplies the data signal for a MLS drive to the signal line of the above-mentioned liquid crystal display panel 10 through the liquid crystal drive circuit 136. In addition, the

page (low) address control circuit 140 has a page (low) address decoder, and makes one WORD line of RAM100 active based on the page address from either the MPU control circuit 120 or the LCD control circuit 130.

[0016] The explanation of each above-mentioned terminal is as follows.

[0017] D7-D0 -- It connects with the data bus of standard MPU (8 bits or 16 bits) by the 8-bit bidirection data bus.

[0018] A0 -- It connects with the least significant bit of the address bus of MPU, when an input is "0", it is shown that D7-D0 are control data, and when an input is "1", it is shown that D7-D0 are indicative datas.

[0019] /RES -- The reversal signal of reset-signal RES is inputted, and initial setting is carried out when an input is "L."

[0020] /CS -- The reversal signal of chip select signal CS is inputted.

[0021] /RD, /WR, C86 -- It is the terminal properly used in the time of 80 system MPU connection and 68 system MPU connection, and the signal which determines a lead, light timing, etc. is inputted.

[0022] M/S -- It is the terminal which chooses the master / SUIREBU operation of two or more signal-line drives IC by which the cascade connection was carried out. The case where the signal-line drive IC is used for the 1st step is master operation, and is set to M/switch terminal =H at this time. The case where the signal-line drive IC is used after the 2nd step is slave operation, and is set to M/switch terminal =L at this time. It is outputting a signal required for a liquid crystal display at the time of master operation, and inputting a required signal into it at a liquid crystal display at the time of slave operation, and, as for the signal-line drive IC, the synchronization of a liquid crystal display system is taken.

[0023] CL -- It is a display clock input/output terminal, a clock is outputted at the time of master operation, and the clock is inputted when it is slave operation.

[0024] FR -- It is the input/output terminal of a liquid crystal alternating current-ized signal, a liquid crystal alternating current-ized signal is outputted at the time of master operation, and when it is slave operation, the liquid crystal alternating current-ized signal is inputted.

[0025] CA -- It is the input/output terminal of a frame-scanning start signal, a frame-scanning start signal is outputted at the time of master operation, and when it is slave operation, the frame-scanning start signal is inputted.

[0026] G/D ... It is the change control terminal of a gradation display and a binary display, and is a binary display in 4 gradation displays and G/D=L in this example at G/D terminal =H.

[0027] OSCs 1-3 -- It is a terminal for operating the internal oscillator circuit 150 in master operation in which the signal-line drive IC is used for the 1st step. In this case, as shown in drawing 1 , the external circuit 50 for an oscillation which consists of Capacitor C is connected with Resistance R, and the oscillation of the clock of f=1/(2.2xCxR) (Hz) is attained from CL terminal. In slave operation for which the signal-line drive IC is used after the 2nd step, the internal oscillator circuit 150 does not operate, but the above-mentioned frequency clock is inputted into it from CL terminal.

[0028] (Explanation of RAM and its circumference circuit) The example of a binary display is explained first.

[0029] It is changed as the memory address space of RAM100 in one signal-line drive IC shows this example to drawing 3 (B) to the 320x240-pixel display address space of the liquid crystal display panel 10 shown in drawing 3 (A), in order to carry out the MLS drive of four-line simultaneous selection. The number of the memory cells of the direction of a column is 320(book) x8(bit) /2(number of ICs) =1280 piece to the number of the memory cells of the direction of a page of the memory address space of drawing 3 (B) being 240(book) /8(bit) =30 piece. In addition, a page address is set to [0, 1, 2--29] in the memory address space of drawing 3 (B). In the direction of a column of drawing 3 (B), in order that this example may perform read/write of data per 1 byte, the number of column addresses is 1280/8=160. In this example, the column address of RAM100 in the 1st-step signal-line drive IC 22 is set to [0, 1, 2, --159]. The column address of RAM100 in the 2nd-step signal-line drive IC 24 is set to [160, 161, --319]. In addition, when the cascade connection of a maximum of four signal-line drives IC is carried out, the maximum of a column address value is set to [639].

[0030] Drawing 4 is the circuit diagram of RAM100 and its circumference circuit, and the memory cell 102 is connected to 30 WORD lines WL1-WL30 and the bit line pairs BL/BL of 1280 trains, respectively.
[0031] 16 bus lines connected to I/O buffer 124 for RAM shown in drawing 2 are connected to the bit line pairs BL/BL of 1280 trains through each column switch 104, as shown in drawing 4 .
[0032] The column address control circuit 122 shown in drawing 2 has 160 column address decoder 122A for turning on and off simultaneously eight column switches 104 connected to the one transfer gate 106 as it is shown in drawing 4 . This each [of a column address] decoder 122A decodes the 10 bits column address from the MPU system control circuit 120, and the 2-bit logic of two external terminals LR0 and LR1, and turns eight column switches 104 on and off simultaneously. Although each column address decoder 122A is common to each signal drive IC as a mask ROM, the setting potential of two external terminals LR0 and LR1 is changed for every signal drive IC. Thereby, each column address of [0-159] can be decoded by the 1st-step signal drive IC 22, and each column address of [160-319] can be decoded by the 2nd-step signal drive IC 24. And if one column decoder [any] 122A to "L" is outputted, with the output "H" of an inverter 108, and the signal "H" of a column control signal (CALCTL), the one transfer gate 106 is turned on and eight column switches 104 connected to it turn on simultaneously.
[0033] The latch circuit 132 shown in drawing 2 has the latch signal SELR, switch 132A turned on and off by its reversal signal / SELR, and gate circuit 132B for a latch which latches the output as it is shown in drawing 4 . when the WORD line WL1 of the 1st line is made active by the page-address control circuit 140 by this composition, the latch signal SELR is made active -- the 1- on the display address space of drawing 3 (A) -- the pixel data connected to the 4th line are latched simultaneously the same -- time a latch reversal signal / SELR is active -- the 5- on the display address space of drawing 3 (A) -- the pixel data connected to the 8th line are latched simultaneously By switching the WORD line by which active is carried out by the page-address control circuit 140, the data of four lines of a memory cell 102 connected to all WORD lines will be latched at a time one by one.
[0034] The decoder circuit 134 shown in drawing 2 is decoded to the signal for the MLS drive of four-line simultaneous selection, and decodes a latch output based on PR (precharge signal of decoding) and FR (liquid crystal alternating current-ized signal) which are shown in drawing 4 , and F1 and F2 (field signal for distinguishing a MLS pattern).
[0035] The liquid crystal drive circuit 136 shown in drawing 2 determines the signal level impressed to a signal line from various voltage as the output of a decoder circuit 134, as shown in drawing 4 .
[0036] Next, the relation between the display address space of the pixel at the time of performing 4 gradation displays and the memory address space of RAM100 in a signal-line drive is explained. In this example, 4 gradation displays and a binary display can switch by G/D terminal setup. As for the pixel in drawing 3 (A), in 4 gradation displays, 2-bit data correspond, respectively. Speaking concretely, to the indicative data on a data bus D [0:7] corresponding to a1-h1 in a binary display, in 4 gradation displays, corresponding to a1 (a1H, a1L)-d1 (d1H, d1L), as shown in drawing 5 (A). Moreover, the memory address space at this time becomes like drawing 5 (B). In a binary display, the column driver of this example has the display memory for 240 lines. Therefore, it will be called 120 lines when performing 4 gradation displays. Others are the same only by display capacity dropping to 1/2. It is arranged so that the 2-bit data expressing 1 pixel may adjoin each other. Since arrangement of data is arranged as are shown in drawing 4 , and ID0, ID4 and ID1, and ID5 and ID2 adjoined in ID6, ID3, and ID7, it needs to change the correspondence relation between external data bus D [0:7] and internal data bus ID [0:7] by a binary display and 4 gradation displays, and is performed in the I/O circuit of drawing 2 . The correspondence-related change method of data is shown in drawing 6 . In this drawing, since the output of the AND gates 300 and 301 is set to L in control terminal CTL=L, the clocked inverter groups 310 and 311 will not operate, but will be in floating. In control terminal CTL=H, in G/D=L (binary display), the output of the AND gate 300 is set to H, the clocked gate group 310 operates, when it is G/D=H (4 gradation displays), the output of the AND gate 301 is set to H, and the clocked gate group 311 operates. Therefore, according to a setup of terminal G/D, the above-mentioned rearrangement is realizable. In

addition, although this drawing expresses only the write-in portion of an indicative data, a read-out portion is also realizable by the same circuitry.

[0037] (Explanation of 4 gradation displays by pulse width modulation) The four-line simultaneous selection drive is used for this example. In a binary display, data of four lines were read for every 1 level period of a liquid crystal display, and output voltage is determined. Since the data for eight lines correspond to one page so that drawing 3 (B) may show, a page changes for every 2 level periods, and changes an a1-d1, or e1-h1 read-out side for every 1 level period. While a page address's changing for every 2 level periods, speaking concretely, ID0-ID3 corresponding to /SELR of drawing 4 (a1-d1 in a binary display) are read in the level period of the first half, ID4-ID7 (e1-h1 in a binary display) are read in the level period of the second half, and output voltage is determined.

[0038] The example of 4 gradation displays by PDM is explained. In 4 gradation displays, as shown in drawing 5 , 1 pixel has the indicative data which is 2 bits. 1-pixel data consist of pairs called (D0, D1), (D2, D3), (D4, D5), and (D6, D7) on the data bus D [0:7]. Among this, D0, D2, D4, and D6 express the weight of low-ranking gradation (if it says by drawing 5 , they will be a1L, b1L, c1L, and d1L), and D1, D3, D5, and D7 express the weight of the gradation of a high order (if it says by drawing 5 , it will be a1H, b1H, c1H, and d1H). A display control divides 1 level period into 1:2, as shown in drawing 7 (B) (temporarily, a short period is made into F period, a long period is made into S period, and it is clearly written in CL pulse that LP and LP2 illustrate), in F period, the level determined by the low rank indicative data of a1 L-d1L is outputted, and the level determined by the high order indicative data of a1 H-d1H is outputted in S period. This control can use the circuitry for a binary display as it is only by changing how reading Display RAM a little. That is, it prepares for the output of F period, and the bit corresponding to /SELR is read from LP2 of the before (the decoded result is latched by LP), it prepares for the output of S period, and the bit corresponding to SELR is read from LP of the before (the decoded result is latched by LP2). The change of /SELR and SELR is performed for every 1 level period, and changes of a page address are performed for every 1 level period. In order to give explanation intelligible, the example of a binary display is also doubled and shown in drawing 7 (A).

[0039] Although this example showed the case where it had the display memory for 120 lines by 4 gradation displays, it is easily realizable if the memory of double precision is prepared in the direction of a page when performing a 240-line display. Moreover, by binary display, 480 lines can be displayed in that case.

[0040] As shown in drawing 7 (B), in 4 gradation displays, CL signal which is illustrated is required. This signal is performed within the LCD control circuit 130 of drawing 2 . That is, the oscillation of one 3 times [at the time of usually performing a binary display] the frequency of this is oscillated by the internal oscillator circuit 150 (a setup to preparation is possible by constant change of C and R), and the generating circuit of this CL signal is shown in drawing 8 . The duty 50% square wave generated in the internal oscillator circuit is inputted into Terminal CLK among drawing, and the pulse which had the width of face of the amount of delay of a DELAY circuit to the standup timing of CLK with the circuit block 320 is generated. The circuit block 330 is a ternary counter which operates by the rising edge of a CLK signal. The output pulse of 320 is controlled by this output, and a wave [as / in drawing 7 (B)] is outputted to Terminal CL.

[0041] Moreover, although this example showed the example which divided 1 level period into 1:2, a change position cannot be determined by only trichotomizing 1 level period, but a change position can be adjusted by dividing 1 level period in more periods. Thereby, according to the optical property of the liquid crystal panel to be used, the high gradation display of reliance display grace becomes realizable. What is necessary is to make it generate the frequency of an internal oscillation in number-of-partitions twice, and just to make a frequency divider etc. into the thing corresponding to it. A frequency divider etc. can be easily guessed from the example of drawing 8 .

[0042]

[Effect of the Invention] In the liquid crystal driving gear which consists of a scanning electrode drive circuit and a signal-electrode drive circuit, and performs the display control by the L line simultaneous selection driving method as explained above A signal-electrode drive circuit has the frame memory and

gradation display-control means for indicative-data storage. The composition whose display RAM of 2L bit is made to correspond to the generation circuit of 1 segment output is taken, by performing read-out operation of every L bits, the RAM composition of this signal-electrode drive circuit is a low power, and the liquid crystal drive of it which can switch a gradation display and the binary display of the number double precision of display pixels is attained.

[Translation done.]

TECHNICAL FIELD

[The technical field to which invention belongs] this invention relates to improvement of the liquid crystal driving gear used for a liquid crystal display.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Conventionally, in the simple matrix liquid crystal display as an example of a flat-panel display, the method using a matrix type liquid crystal display element module controller (henceforth a module controller) as a method which transmits an indicative data to a LCD module (it consists of a liquid crystal display panel, a scanning electrode drive circuit, a signal-electrode drive circuit, etc.) from the MPU (microprocessor unit) side is typical. This method reads an indicative data from the Video RAM (VRAM) the module controller connected with a system bus like the display which used CRT has remembered the indicative data to be, transmits this with the clock of high frequency to a LCD module, and display refreshment operation is performed. In case a gradation display is performed in such a LCD module, usually, a module controller performs a gradation display control, changes into a binary signal to a signal-electrode drive circuit, and the indicative data is transmitted.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] In the liquid crystal driving gear which consists of a scanning electrode drive circuit and a signal-electrode drive circuit, and performs the display control by the L line simultaneous selection driving method as explained above A signal-electrode drive circuit has the frame memory and gradation display-control means for indicative-data storage, and the RAM composition of this signal-electrode drive circuit takes the composition which makes the display RAM of 2L bit correspond to the generation circuit of 1 segment output, and by performing read-out operation of every L bits, it is a low power and becomes that the liquid crystal drive which can switch a gradation display and the binary display of the number double precision of display pixels is possible.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, since read-out from a video ram (it is called Following VRAM) and a transfer are performed in accordance with liquid crystal display timing, in the above-mentioned conventional example, it is usually necessary to always operate VRAM, a module controller, and a liquid crystal driver by the high-frequency clock of several MHz, and to have a RF generating circuit for it in a module controller. Moreover, penetration current etc. arises in much CMOS with which VRAM, a module controller, and a liquid crystal driver are covered, and the circuit related to this operation of a series of constitutes a circuit element according to operation of the large-scale circuit in this high-frequency clock, and it leads to increase of power consumption, and if a large-sized LCD panel is used, it will increase so much. Furthermore, since a transfer clock goes up as compared with a binary display when performing a gradation display, the further increase of power consumption is caused.
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MEANS

[Means for Solving the Problem] In order to solve the above-mentioned technical problem, the means which this invention provided builds in display memory in a signal-electrode drive circuit (column driver), and is characterized by the form to which the column driver was made to carry out the gradation display control itself.
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[The form of operation of this invention] Hereafter, this invention is concretely explained with reference to a drawing about the form of operation of the adapted liquid crystal driving gear.
[0007] (Explanation of the control system of the whole equipment) Drawing 1 shows the general drawing of the liquid crystal driving gear containing a liquid crystal display panel. In drawing 1 , the liquid crystal display panel 10 is equipped with the pixel of 320x240, a switching element and a liquid crystal layer are connected to the pixel position formed of intersection with 320 signal lines and the 240 scanning lines in series, and a pixel is constituted. In addition, let the liquid crystal display panel 10 be the active matrix type liquid crystal display panel which connected to each liquid crystal layer of a pixel position 3 terminal type switching element represented with TFT, or 2 terminal type switching element represented by MIM. Or you may be a simple matrix type liquid crystal display panel.
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[0010] The scanning-line driver (low driver) 30 supplies a scanning signal to the 240 scanning lines, and has the 1st scanning-line drive IC 32 and the 2nd scanning-line drive IC 34 in this example. The 1st scanning-line drive IC 32 supplies a scanning signal to one to 120 Motome's scanning line, and the 2nd scanning-line drive IC 34 supplies a scanning signal to 121 to 240 Motome's scanning line.
[0011] Power is supplied to the signal-line driver 20 and the scanning-line driver 30 from a power circuit 40, and various command signals and a data signal are supplied to them from a microprocessing unit (MPU) 60.

[0012] (Explanation of the signal-line drive IC) Next, the detail of the 1st which both has the same composition, and 2nd signal-line drive 22 and ICs 24 is explained with reference to drawing 2 .
[0013] Drawing 2 shows composition common to the signal-line drive IC. With indicative-data RAM100 and the MPU control circuit 120 which controls read/write operation of an indicative data per 1 byte as opposed to this indicative-data RAM100, from indicative-data RAM100, the indicative data for four lines is read and controlled, and this signal-line drive IC has the LCD control circuit 130 which enables the MLS (multi-line selection) drive of four-line simultaneous selection. /CS, A0, /RD, /WR, C86, and /RES are connected to the bus line 111 inside IC through the MPU interface 110 as a terminal for bus connections. Moreover, D7-D0 are further connected to this bus line 100 through the I/O circuit 112 as a terminal for bus connections. The control data and the indicative data which are outputted and inputted through the MPU interface 110 and the I/O circuit 112 can be held by the bus holder 114 through a bus line 111. Control data is decoded by the command decoder 116, and is used as a command signal to the status setting circuit 118 and the MPU control circuit 120.
[0014] The MPU control circuit 120 controls the column address control circuit 122 and I/O buffer 124 for RAM, and carries out read/write of the indicative data to RAM100 per 1 byte.
[0015] Moreover, it connects with external terminal G/D, FR, CL and CA, and M/S, and the LCD control circuit 130 is connected with the internal oscillator circuit 150. This LCD control circuit 130 carries out drive control of a latch circuit 132 and the decoding circuit 134, reads the indicative data for four lines from RAM100, and supplies the data signal for a MLS drive to the signal line of the above-mentioned liquid crystal display panel 10 through the liquid crystal drive circuit 136. In addition, the page (low) address control circuit 140 has a page (low) address decoder, and makes one WORD line of RAM100 active based on the page address from either the MPU control circuit 120 or the LCD control circuit 130.
[0016] The explanation of each above-mentioned terminal is as follows.
[0017] D7-D0 -- It connects with the data bus of standard MPU (8 bits or 16 bits) by the 8-bit bidirection data bus.
[0018] A0 -- It connects with the least significant bit of the address bus of MPU, when an input is "0", it is shown that D7-D0 are control data, and when an input is "1", it is shown that D7-D0 are indicative datas.
[0019] /RES -- The reversal signal of reset-signal RES is inputted, and initial setting is carried out when an input is "L."
[0020] /CS -- The reversal signal of chip select signal CS is inputted.
[0021] /RD, /WR, C86 -- It is the terminal properly used in the time of 80 system MPU connection and 68 system MPU connection, and the signal which determines a lead, light timing, etc. is inputted.
[0022] M/S -- It is the terminal which chooses the master / SUIREBU operation of two or more signal-line drives IC by which the cascade connection was carried out. The case where the signal-line drive IC is used for the 1st step is master operation, and is set to M/switch terminal =H at this time. The case where the signal-line drive IC is used after the 2nd step is slave operation, and is set to M/switch terminal =L at this time. It is outputting a signal required for a liquid crystal display at the time of master operation, and inputting a required signal into it at a liquid crystal display at the time of slave operation, and, as for the signal-line drive IC, the synchronization of a liquid crystal display system is taken.
[0023] CL -- It is a display clock input/output terminal, a clock is outputted at the time of master operation, and the clock is inputted when it is slave operation.
[0024] FR -- It is the input/output terminal of a liquid crystal alternating current-ized signal, a liquid crystal alternating current-ized signal is outputted at the time of master operation, and when it is slave operation, the liquid crystal alternating current-ized signal is inputted.
[0025] CA -- It is the input/output terminal of a frame-scanning start signal, a frame-scanning start signal is outputted at the time of master operation, and when it is slave operation, the frame-scanning start signal is inputted.
[0026] G/D ... It is the change control terminal of a gradation display and a binary display, and is a binary display in 4 gradation displays and G/D=L in this example at G/D terminal =H.

[0027] OSCs 1-3 -- It is a terminal for operating the internal oscillator circuit 150 in master operation in which the signal-line drive IC is used for the 1st step. In this case, as shown in drawing 1 , the external circuit 50 for an oscillation which consists of Capacitor C is connected with Resistance R, and the oscillation of the clock of f=1/(2.2xCxR) (Hz) is attained from CL terminal. In slave operation for which the signal-line drive IC is used after the 2nd step, the internal oscillator circuit 150 does not operate, but the above-mentioned frequency clock is inputted into it from CL terminal.
[0028] (Explanation of RAM and its circumference circuit) The example of a binary display is explained first.
[0029] It is changed as the memory address space of RAM100 in one signal-line drive IC shows this example to drawing 3 (B) to the 320x240-pixel display address space of the liquid crystal display panel 10 shown in drawing 3 (A), in order to carry out the MLS drive of four-line simultaneous selection. The number of the memory cells of the direction of a column is 320(book) x8(bit) /2(number of ICs) =1280 piece to the number of the memory cells of the direction of a page of the memory address space of drawing 3 (B) being 240(book) /8(bit) =30 piece. In addition, a page address is set to [0, 1, 2--29] in the memory address space of drawing 3 (B). In the direction of a column of drawing 3 (B), in order that this example may perform read/write of data per 1 byte, the number of column addresses is 1280/8=160. In this example, the column address of RAM100 in the 1st-step signal-line drive IC 22 is set to [0, 1, 2, --159]. The column address of RAM100 in the 2nd-step signal-line drive IC 24 is set to [160, 161, --319]. In addition, when the cascade connection of a maximum of four signal-line drives IC is carried out, the maximum of a column address value is set to [639].
[0030] Drawing 4 is the circuit diagram of RAM100 and its circumference circuit, and the memory cell 102 is connected to 30 WORD lines WL1-WL30 and the bit line pairs BL/BL of 1280 trains, respectively.
[0031] 16 bus lines connected to I/O buffer 124 for RAM shown in drawing 2 are connected to the bit line pairs BL/BL of 1280 trains through each column switch 104, as shown in drawing 4 .
[0032] The column address control circuit 122 shown in drawing 2 has 160 column address decoder 122A for turning on and off simultaneously eight column switches 104 connected to the one transfer gate 106 as it is shown in drawing 4 . This each [of a column address] decoder 122A decodes the 10 bits column address from the MPU system control circuit 120, and the 2-bit logic of two external terminals LR0 and LR1, and turns eight column switches 104 on and off simultaneously. Although each column address decoder 122A is common to each signal drive IC as a mask ROM, the setting potential of two external terminals LR0 and LR1 is changed for every signal drive IC. Thereby, each column address of [0-159] can be decoded by the 1st-step signal drive IC 22, and each column address of [160-319] can be decoded by the 2nd-step signal drive IC 24. And if one column decoder [any] 122A to "L" is outputted, with the output "H" of an inverter 108, and the signal "H" of a column control signal (CALCTL), the one transfer gate 106 is turned on and eight column switches 104 connected to it turn on simultaneously.
[0033] The latch circuit 132 shown in drawing 2 has the latch signal SELR, switch 132A turned on and off by its reversal signal / SELR, and gate circuit 132B for a latch which latches the output as it is shown in drawing 4 . when the WORD line WL1 of the 1st line is made active by the page-address control circuit 140 by this composition, the latch signal SELR is made active -- the 1- on the display address space of drawing 3 (A) -- the pixel data connected to the 4th line are latched simultaneously Similarly, when a latch reversal signal / SELR is active, the pixel data connected to the 5th - the octavus line on the display address space of drawing 3 (A) are latched simultaneously. By switching the WORD line by which active is carried out by the page-address control circuit 140, the data of four lines of a memory cell 102 connected to all WORD lines will be latched at a time one by one.
[0034] The decoder circuit 134 shown in drawing 2 is decoded to the signal for the MLS drive of four-line simultaneous selection, and decodes a latch output based on PR (precharge signal of decoding) and FR (liquid crystal alternating current-ized signal) which are shown in drawing 4 , and F1 and F2 (field signal for distinguishing a MLS pattern).
[0035] The liquid crystal drive circuit 136 shown in drawing 2 determines the signal level impressed to a

signal line from various voltage as the output of a decoder circuit 134, as shown in drawing 4 .
[0036] Next, the relation between the display address space of the pixel at the time of performing 4 gradation displays and the memory address space of RAM100 in a signal-line drive is explained. In this example, 4 gradation displays and a binary display can switch by G/D terminal setup. As for the pixel in drawing 3 (A), in 4 gradation displays, 2-bit data correspond, respectively. Speaking concretely, to the indicative data on a data bus D [0:7] corresponding to a1-h1 in a binary display, in 4 gradation displays, corresponding to a1 (a1H, a1L)-d1 (d1H, d1L), as shown in drawing 5 (A). Moreover, the memory address space at this time becomes like drawing 5 (B). In a binary display, the column driver of this example has the display memory for 240 lines. Therefore, it will be called 120 lines when performing 4 gradation displays. Others are the same only by display capacity dropping to 1/2. It is arranged so that the 2-bit data expressing 1 pixel may adjoin each other. Since arrangement of data is arranged as are shown in drawing 4 , and ID0, ID4 and ID1, and ID5 and ID2 adjoined in ID6, ID3, and ID7, it needs to change the correspondence relation between external data bus D [0:7] and internal data bus ID [0:7] by a binary display and 4 gradation displays, and is performed in the I/O circuit of drawing 2 . The correspondence-related change method of data is shown in drawing 6 . In this drawing, since the output of the AND gates 300 and 301 is set to L in control terminal CTL=L, the clocked inverter groups 310 and 311 will not operate, but will be in floating. In control terminal CTL=H, in G/D=L (binary display), the output of the AND gate 300 is set to H, the clocked gate group 310 operates, when it is G/D=H (4 gradation displays), the output of the AND gate 301 is set to H, and the clocked gate group 311 operates. Therefore, according to a setup of terminal G/D, the above-mentioned rearrangement is realizable. In addition, although this drawing expresses only the write-in portion of an indicative data, a read-out portion is also realizable by the same circuitry.
[0037] (Explanation of 4 gradation displays by pulse width modulation) The four-line simultaneous selection drive is used for this example. In a binary display, data of four lines were read for every 1 level period of a liquid crystal display, and output voltage is determined. Since the data for eight lines correspond to one page so that drawing 3 (B) may show, a page changes for every 2 level periods, and changes an a1-d1, or e1-h1 read-out side for every 1 level period. While a page address's changing for every 2 level periods, speaking concretely, ID0-ID3 corresponding to /SELR of drawing 4 (a1-d1 in a binary display) are read in the level period of the first half, ID4-ID7 (e1-h1 in a binary display) are read in the level period of the second half, and output voltage is determined.
[0038] The example of 4 gradation displays by PDM is explained. In 4 gradation displays, as shown in drawing 5 , 1 pixel has the indicative data which is 2 bits. 1-pixel data consist of pairs called (D0, D1), (D2, D3), (D4, D5), and (D6, D7) on the data bus D [0:7]. Among this, D0, D2, D4, and D6 express the weight of low-ranking gradation (if it says by drawing 5 , they will be a1L, b1L, c1L, and d1L), and D1, D3, D5, and D7 express the weight of the gradation of a high order (if it says by drawing 5 , it will be a1H, b1H, c1H, and d1H). A display control divides 1 level period into 1:2, as shown in drawing 7 (B) (temporarily, a short period is made into F period, a long period is made into S period, and it is clearly written in CL pulse that LP and LP2 illustrate), in F period, the level determined by the low rank indicative data of a1 L-d1L is outputted, and the level determined by the high order indicative data of a1 H-d1H is outputted in S period. This control can use the circuitry for a binary display as it is only by changing how reading Display RAM a little. That is, it prepares for the output of F period, and the bit corresponding to /SELR is read from LP2 of the before (the decoded result is latched by LP), it prepares for the output of S period, and the bit corresponding to SELR is read from LP of the before (the decoded result is latched by LP2). The change of /SELR and SELR is performed for every 1 level period, and changes of a page address are performed for every 1 level period. In order to give explanation intelligible, the example of a binary display is also doubled and shown in drawing 7 (A).
[0039] Although this example showed the case where it had the display memory for 120 lines by 4 gradation displays, it is easily realizable if the memory of double precision is prepared in the direction of a page when performing a 240-line display. Moreover, by binary display, 480 lines can be displayed in that case.
[0040] As shown in drawing 7 (B), in 4 gradation displays, CL signal which is illustrated is required.

This signal is performed within the LCD control circuit 130 of drawing 2 . That is, the oscillation of one 3 times [at the time of usually performing a binary display] the frequency of this is oscillated by the internal oscillator circuit 150 (a setup to preparation is possible by constant change of C and R), and the generating circuit of this CL signal is shown in drawing 8 . The duty 50% square wave generated in the internal oscillator circuit is inputted into Terminal CLK among drawing, and the pulse which had the width of face of the amount of delay of a DELAY circuit to the standup timing of CLK with the circuit block 320 is generated. The circuit block 330 is a ternary counter which operates by the rising edge of a CLK signal. The output pulse of 320 is controlled by this output, and a wave [as / in drawing 7 (B)] is outputted to Terminal CL.

[0041] Moreover, although this example showed the example which divided 1 level period into 1:2, a change position cannot be determined by only trichotomizing 1 level period, but a change position can be adjusted by dividing 1 level period in more periods. Thereby, according to the optical property of the liquid crystal panel to be used, the high gradation display of reliance display grace becomes realizable. What is necessary is to make it generate the frequency of an internal oscillation in number-of-partitions twice, and just to make a frequency divider etc. into the thing corresponding to it. A frequency divider etc. can be easily guessed from the example of drawing 8 .

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the liquid crystal display which applied this invention.
[Drawing 2] It is the block diagram showing the composition of a signal-line driver shown in drawing 1 .
[Drawing 3] (A) is outline explanatory drawing showing the operating-space address in the binary display of the liquid crystal display panel of drawing 1 , and (B) is outline explanatory drawing showing the pixel address of RAM in the signal-line drive IC shown in drawing 1 .
[Drawing 4] It is the circuit diagram showing RAM shown in drawing 2 , and its circumference circuit.
[Drawing 5] (A) is outline explanatory drawing showing the operating-space address in 4 gradation displays of the liquid crystal display panel of drawing 1 , and (B) is outline explanatory drawing showing the pixel address of RAM in the signal-line drive IC shown in drawing 1 .
[Drawing 6] It is the correspondence relation change circuit of a data bus and an internal bus.
[Drawing 7] (A) is the timing chart showing the read-out timing of RAM in a binary display, and (B) is the timing chart showing the read-out timing of RAM in 4 gradation displays by PDM.
[Drawing 8] It is CL generating circuit in 4 gradation displays by PDM.
[Description of Notations]
10 Liquid Crystal Display Panel
20 Signal-Line Driver
22 1st Signal-Line Drive IC
24 2nd Signal-Line Drive IC
30 Scanning-Line Driver
32 34 Scanning-line drive IC
40 Power Circuit
50 External Circuit for Oscillation
60 MPU
100 Indicative-Data RAM
102 Memory Cell
104 Column Switch
106 Transfer Gate
108 Inverter
110 MPU Interface
111 Bus Line
112 I/O Circuit
114 Bus Holder
116 Command Decoder
118 Status Setting Circuit
120 MPU Control Circuit
120A Clock control circuit

122 Column Address Control Circuit
122A Column address decoder
123A Column address decoder circuit
123B Column address counter circuit
124 I/O Buffer
130 LCD Control Circuit
132 Latch Circuit
134 Decoding Circuit
136 Liquid Crystal Drive Circuit
140 Page-Address Control Circuit
140A Page (low) address decoder circuit
140B Page-address counter circuit
150 Internal Oscillator Circuit
200 Monitor Circuit
202 N Type Transistor
204 Common Path Cord
206 Inverter for Monitors
210 Precharge Circuit
212 Transfer Gate
214,216 P type transistor
300 301 AND gate
310 311 Clocked inverter
320 Pulse Generator
330 CLK Counter Circuit
340 AND Gate

[Translation done.]

* NOTICES *

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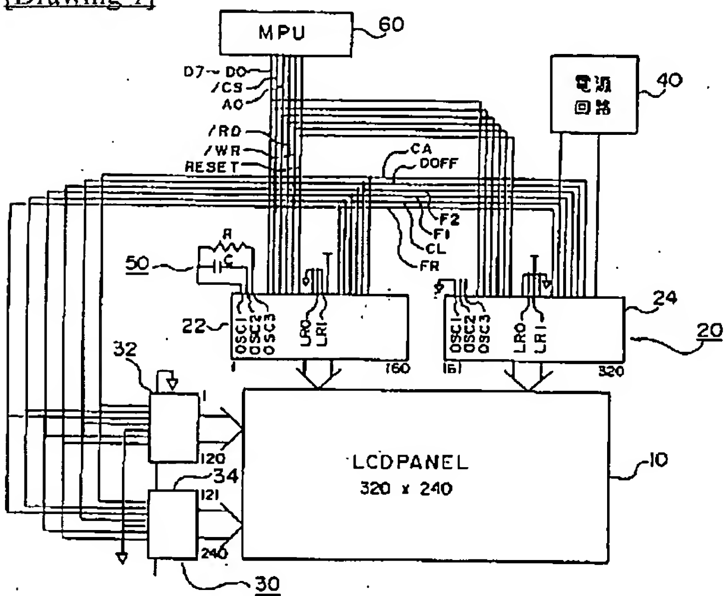
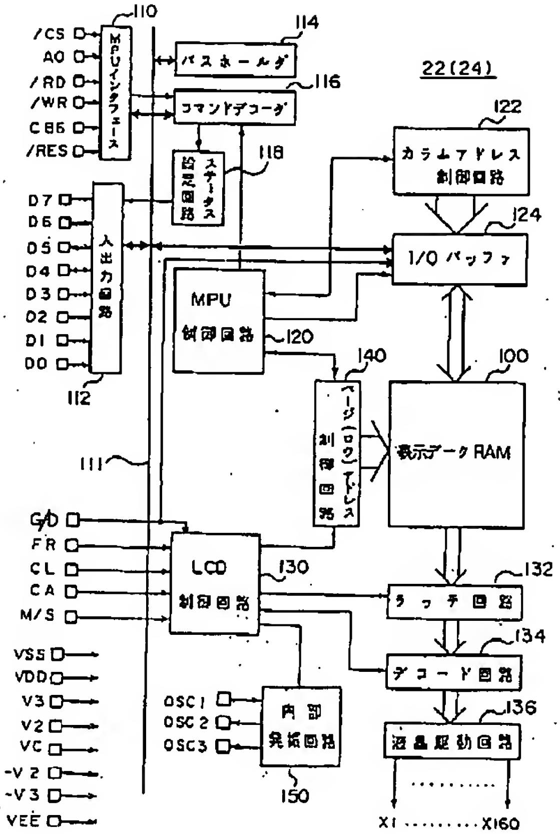
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

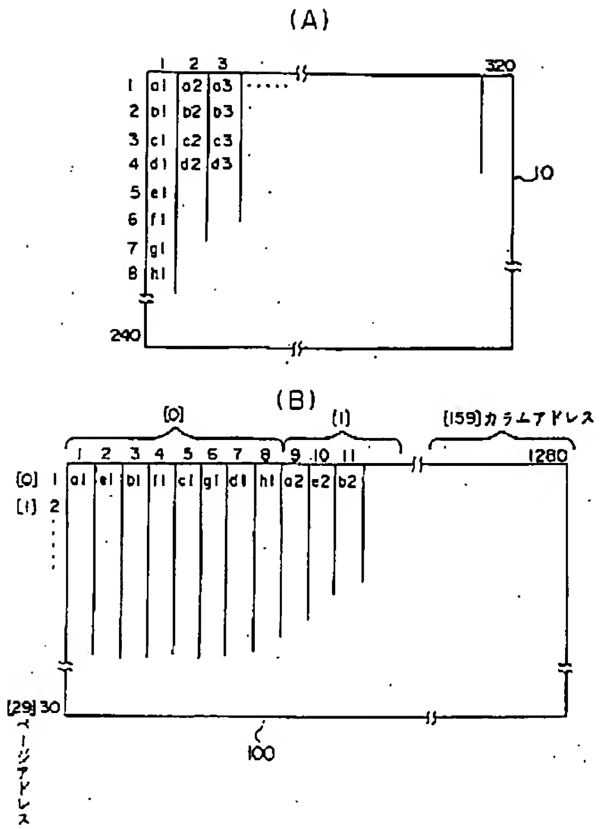


[Drawing 2]

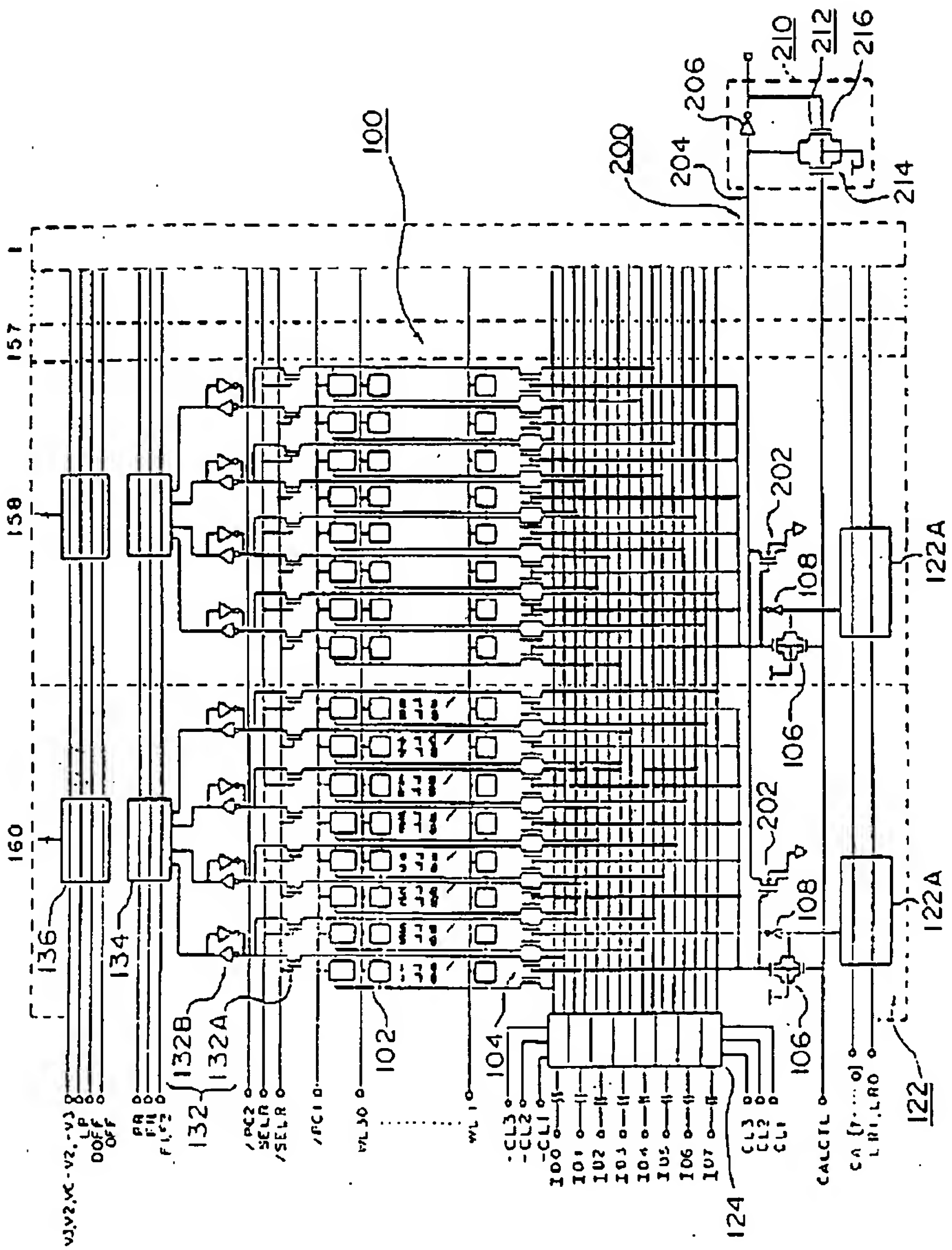


22(24)
110
114
116
118
122
124
120
140
100
112
111
130
132
134
136
150
/CS
A0
/RD
/WR
C86
/RES
MPUインタフェース
バスホールダ
コマンドデコーダ
ステータス設定回路
カラムアドレス制御回路
I/Oバッファ
D7
D6
D5
D4
D3
D2
D1
D0
入出力回路
MPU
制御回路
ページ(ロウ)アドレス制御回路
表示データRAM
FR
CL
CA
M/S
LCD
制御回路
ラッチ回路
デコード回路
液晶駆動回路
VSS
VDD
V3
V2
VC
-V2
-V3
VEE
OSC1
OSC2
OSC3
内部
発振回路
X1 .... X160

[Drawing 3]

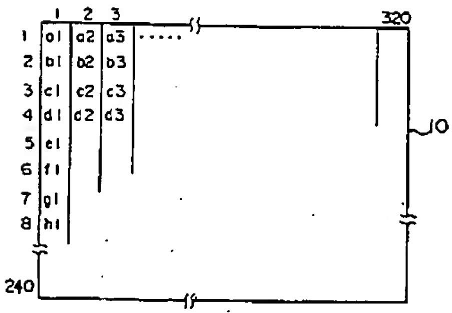


[Drawing 4]

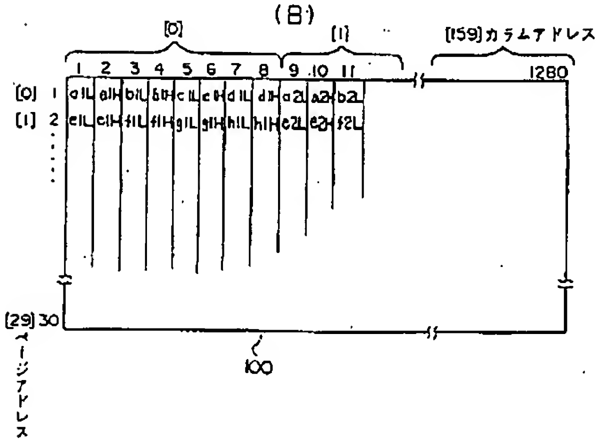

100
200
204
206
210
212
216
214
157
158
160
136
134
132B
132A
132
102
104
202
108
106
122A
122
124
CALCTL

[Drawing 5]

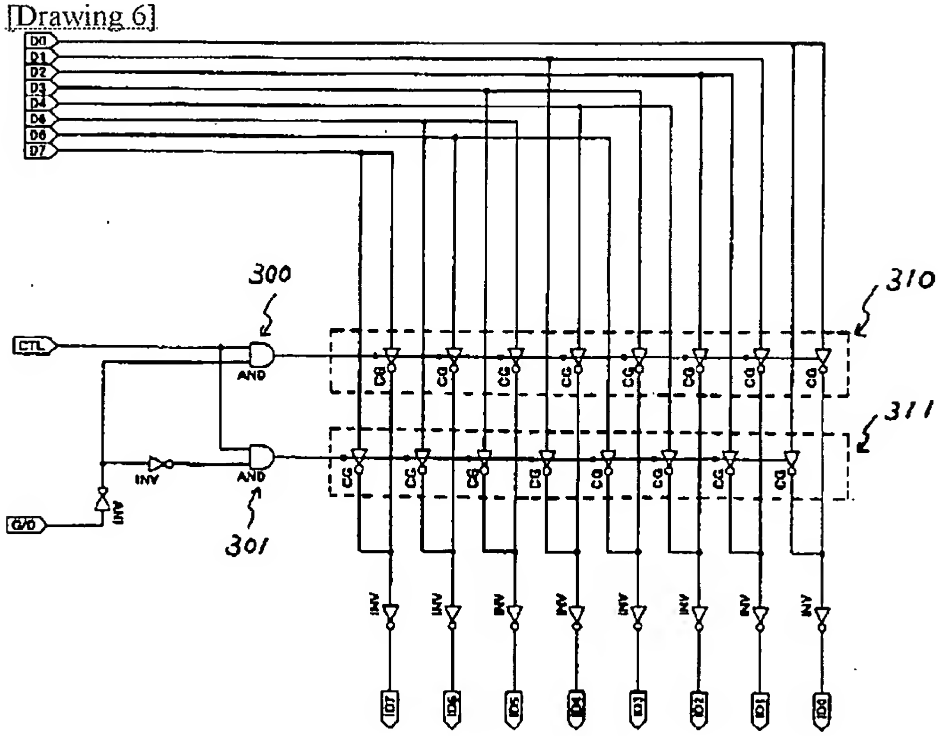
(A)



(B)

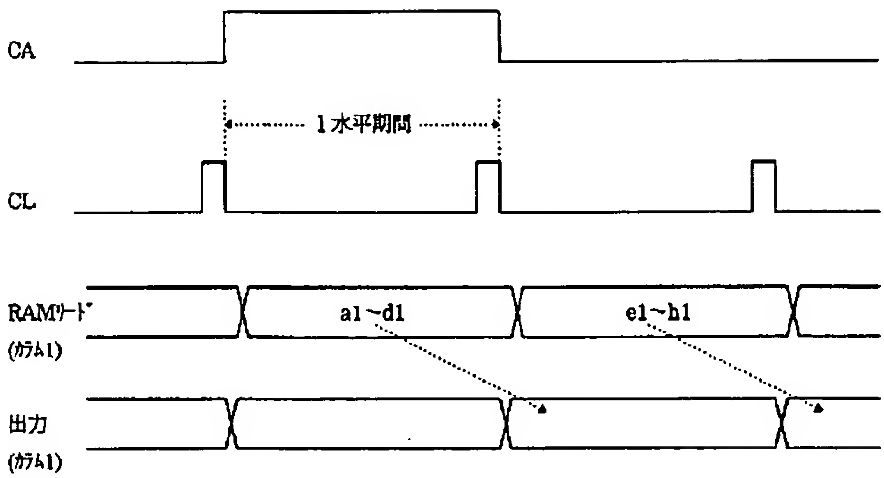


[Drawing 6]

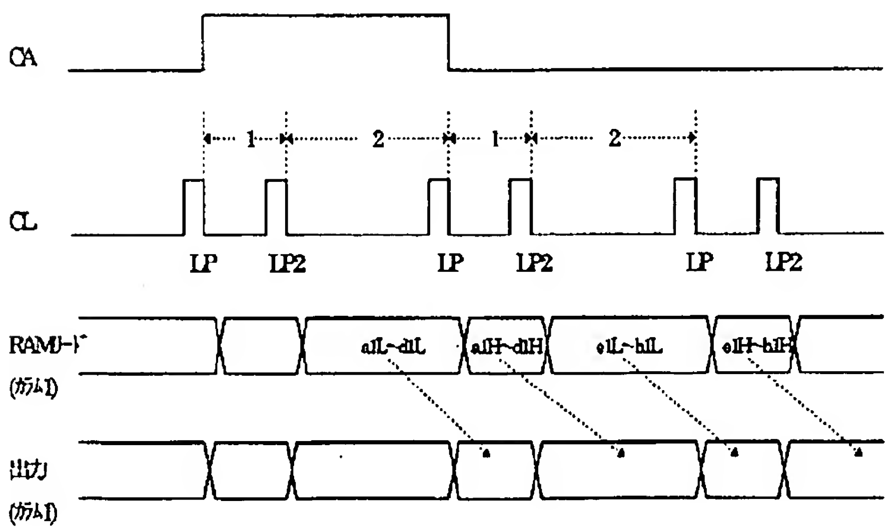


[Drawing 7]

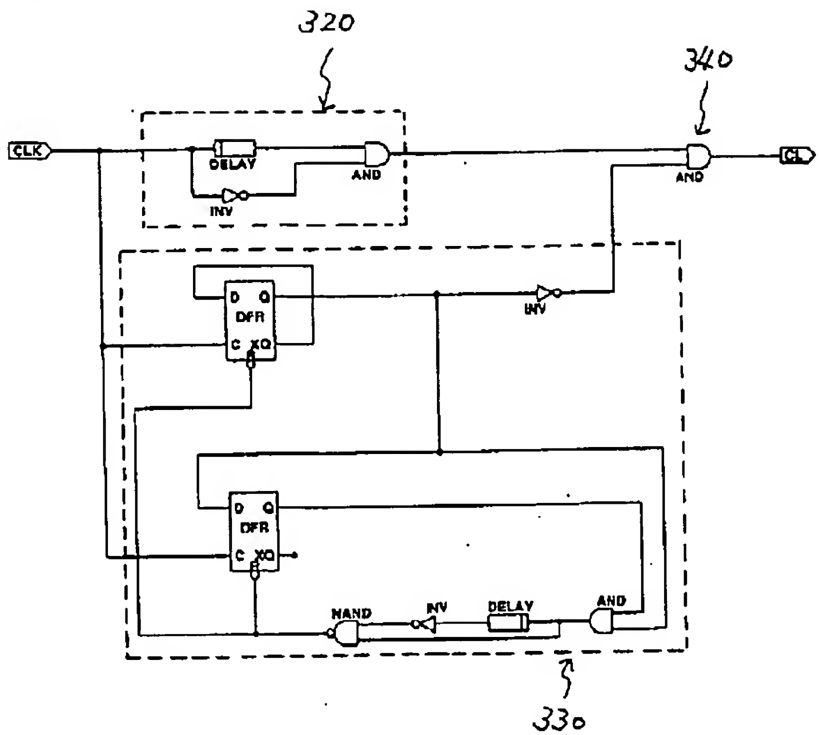
(A)


CA
1水平期間
CL
RAMリード
(カラム1)
a1~d1
e1~h1
出力
(カラム1)

(B)


CA
1
2
1
2
CL
LP
LP2
LP
LP2
LP
LP2
RAMリード
(カラム1)
a1L~d1L
a1H~d1H
e1L~h1L
e1H~h1H
出力
(カラム1)

[Drawing 8]



[Translation done.]